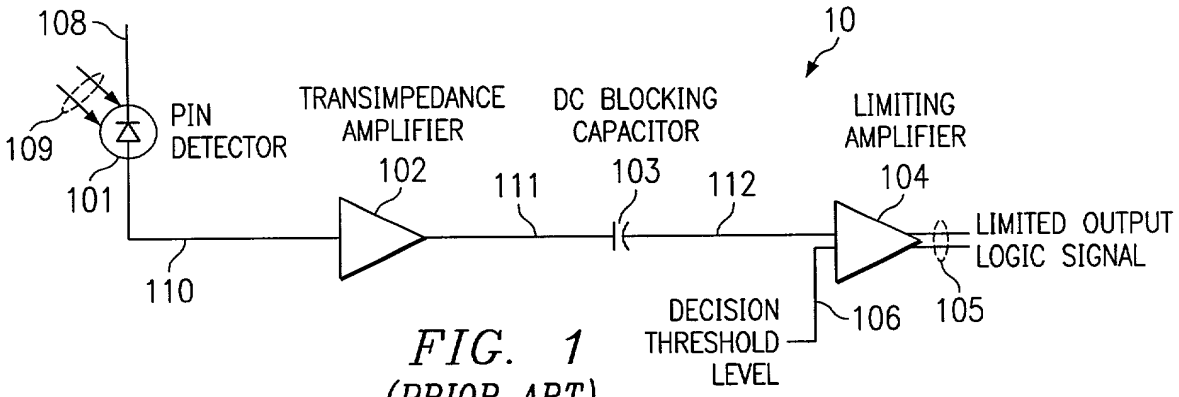


FIG. 1
(PRIOR ART)

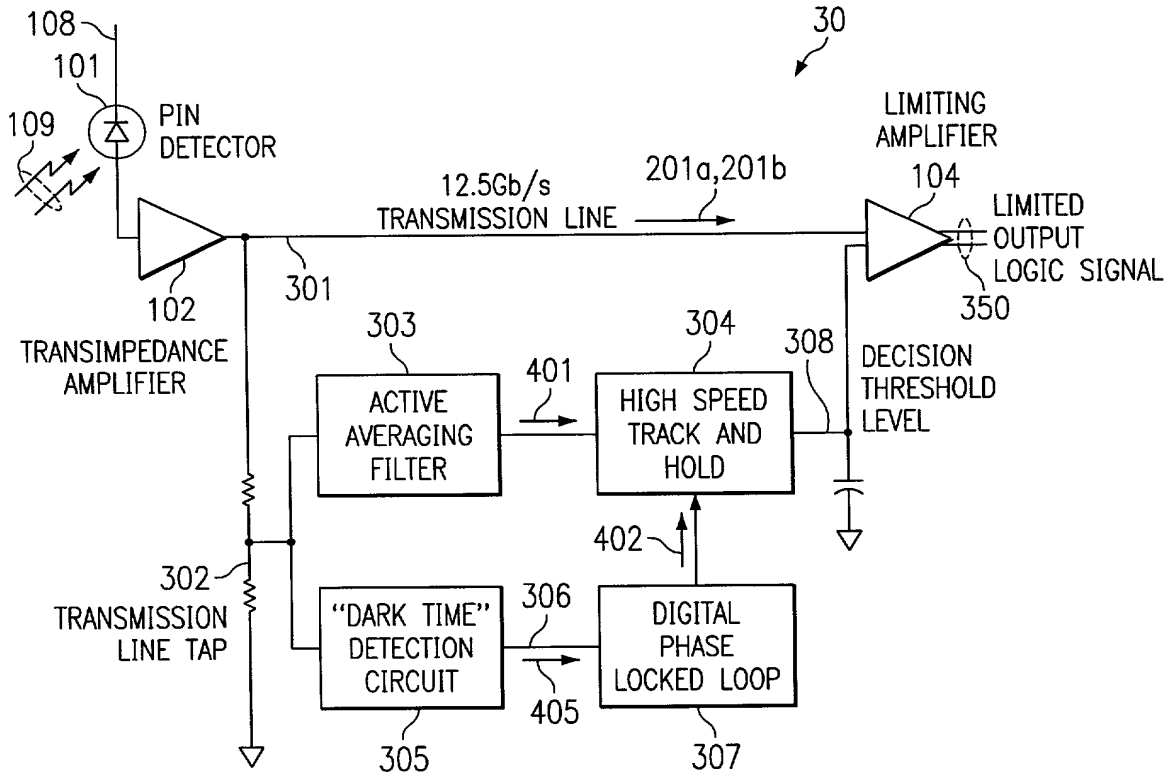


FIG. 3

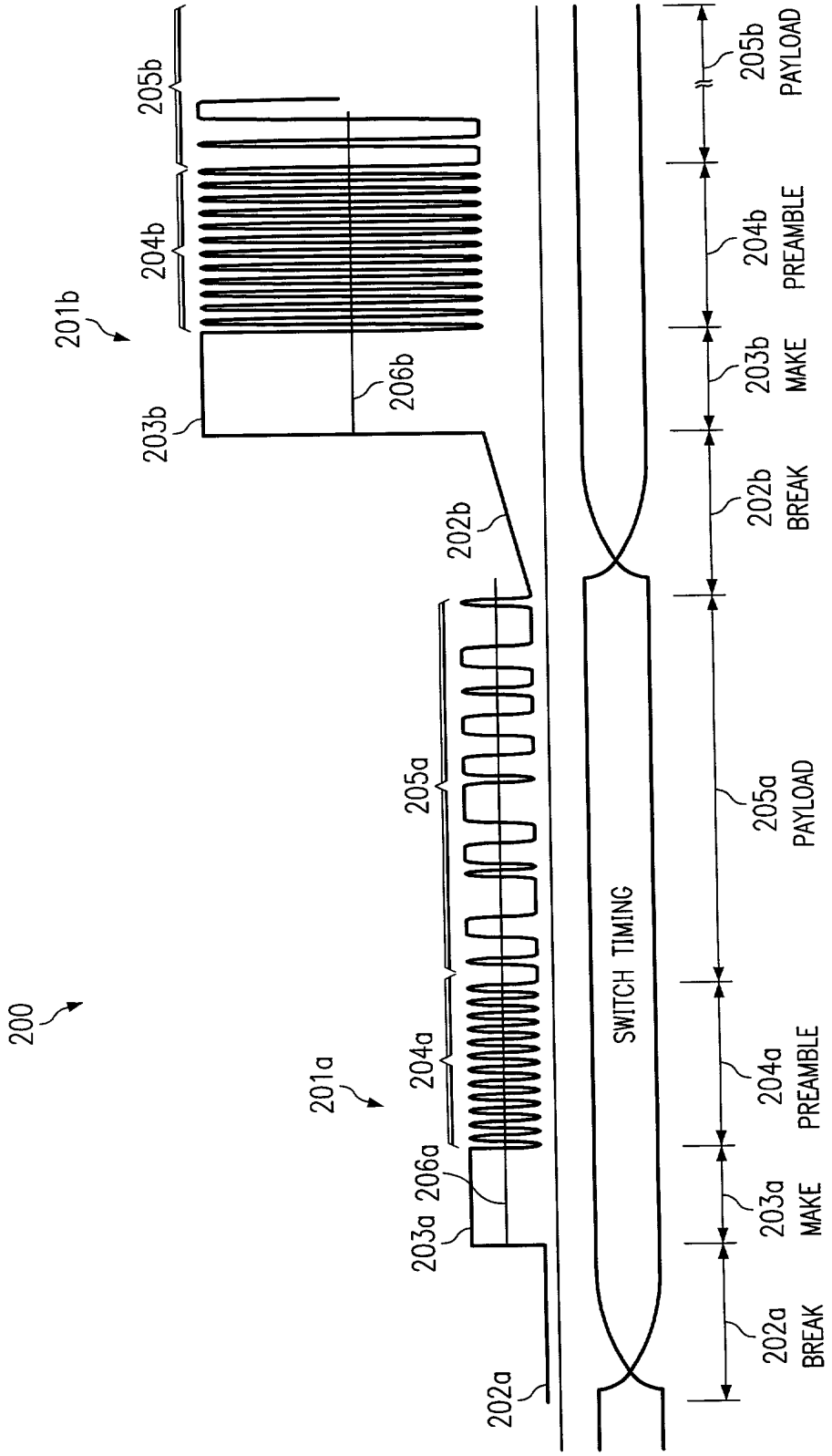

200
201a
201b
202a
202b
203a
203b
204a
204b
205a
205b
206a
206b
SWITCH TIMING
BREAK
MAKE
PREAMBLE
PAYLOAD

FIG. 2

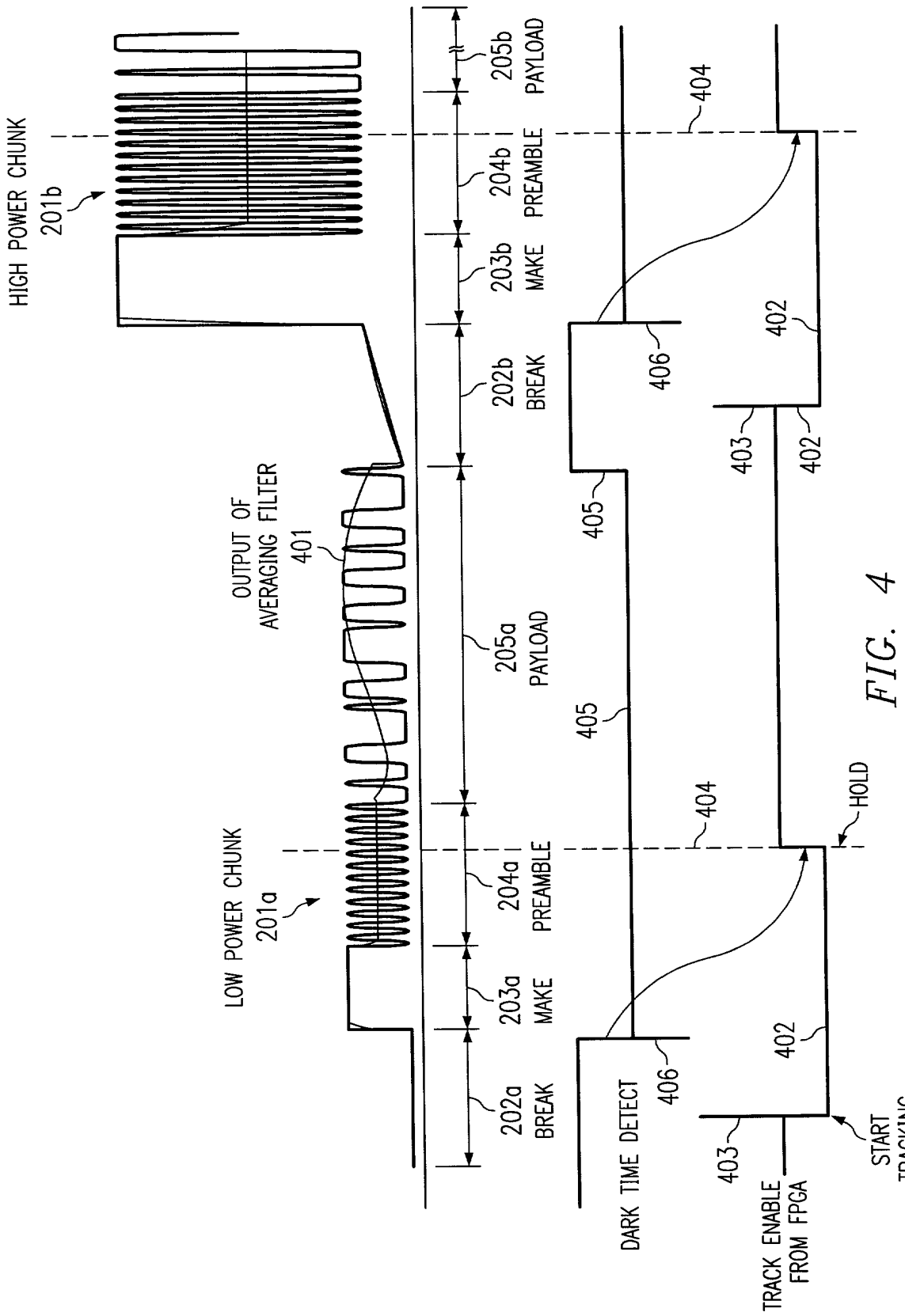

HIGH POWER CHUNK
201b
LOW POWER CHUNK
201a
OUTPUT OF AVERAGING FILTER
401
202a BREAK
203a MAKE
204a PREAMBLE
205a PAYLOAD
202b BREAK
203b MAKE
204b PREAMBLE
205b PAYLOAD
404
405
406
402
403
DARK TIME DETECT
TRACK ENABLE FROM FPGA
START TRACKING
HOLD

FIG. 4

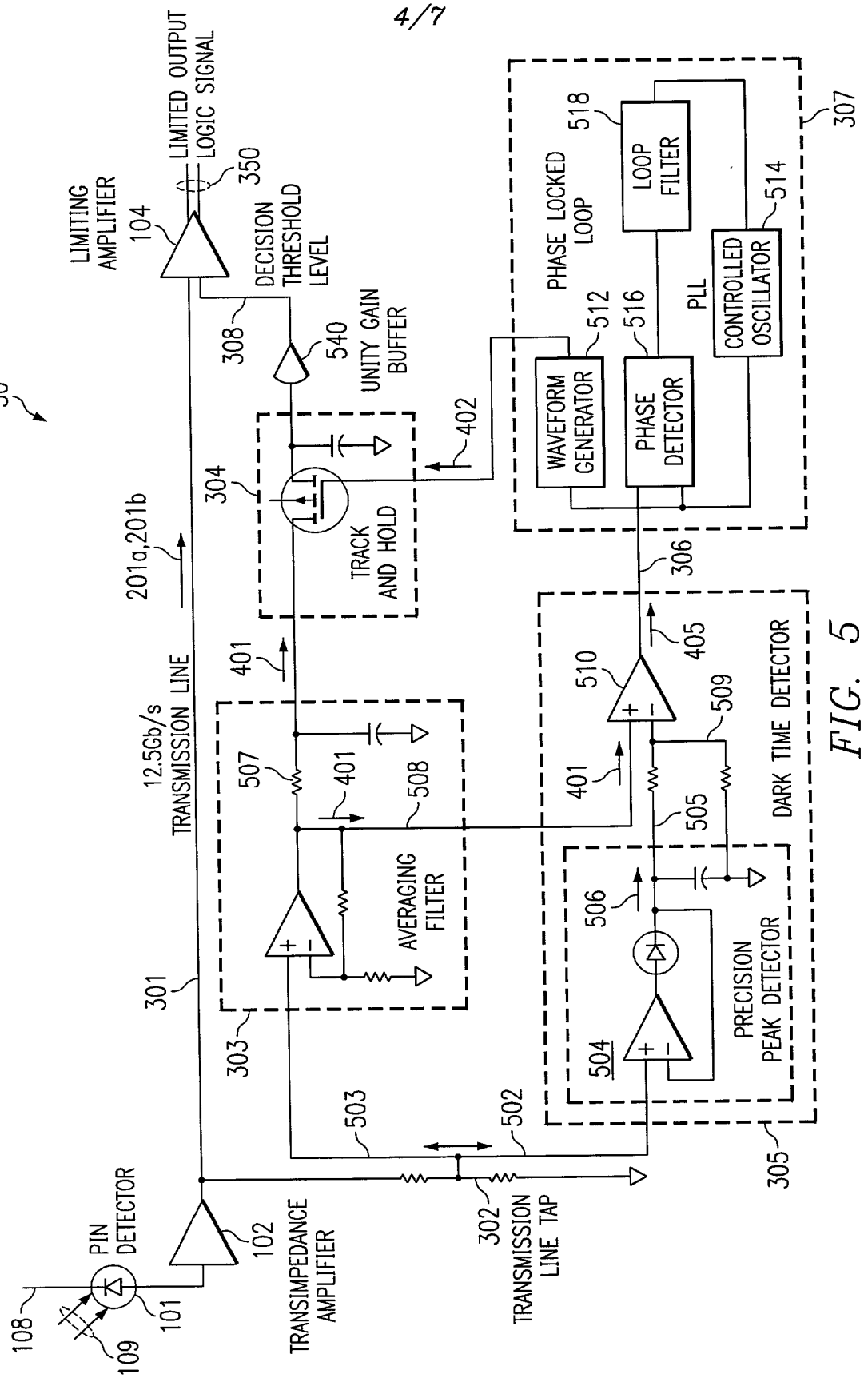

30
108
109
PIN DETECTOR
101
102
TRANSIMPEDANCE AMPLIFIER
LIMITING AMPLIFIER
104
LIMITED OUTPUT LOGIC SIGNAL
350
DECISION THRESHOLD LEVEL
308
540
UNITY GAIN BUFFER
402
304
TRACK AND HOLD
201a,201b
12.5Gb/s TRANSMISSION LINE
301
303
401
507
508
AVERAGING FILTER
503
502
302
TRANSMISSION LINE TAP
PHASE LOCKED LOOP
307
WAVEFORM GENERATOR
512
PHASE DETECTOR
516
PLL
CONTROLLED OSCILLATOR
514
LOOP FILTER
518
306
405
510
509
505
506
504
PRECISION PEAK DETECTOR
DARK TIME DETECTOR
305

FIG. 5

FIG. 6

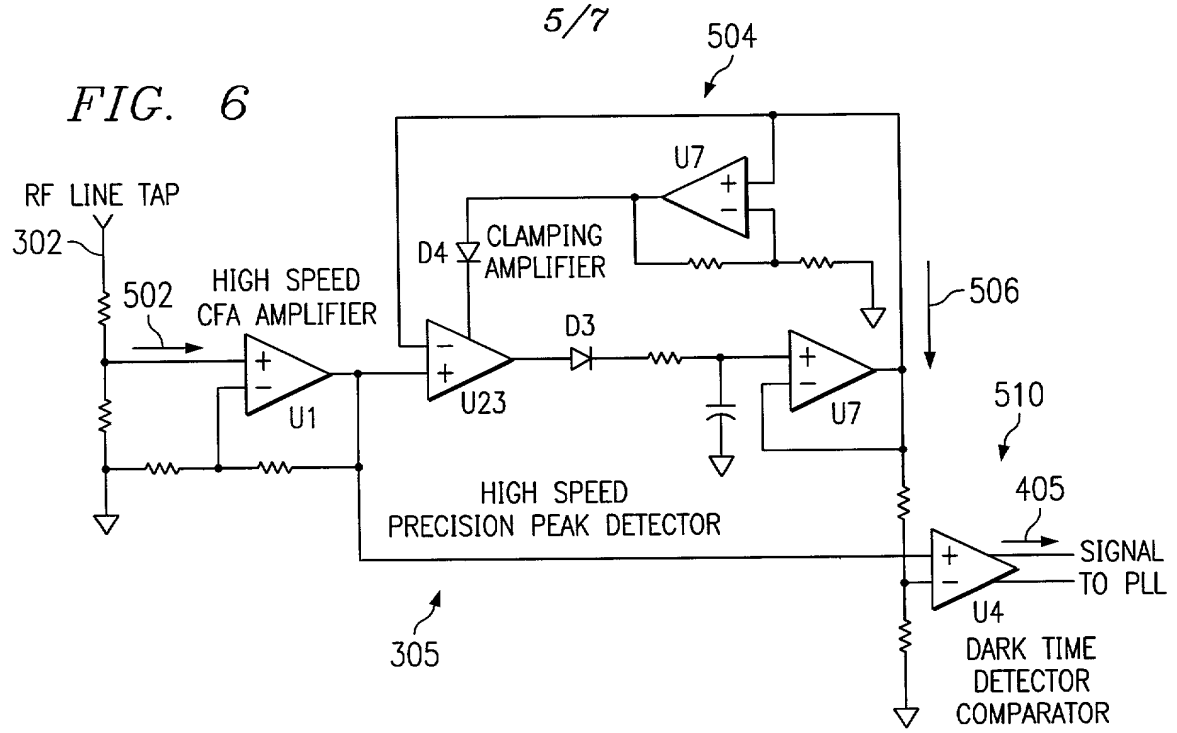
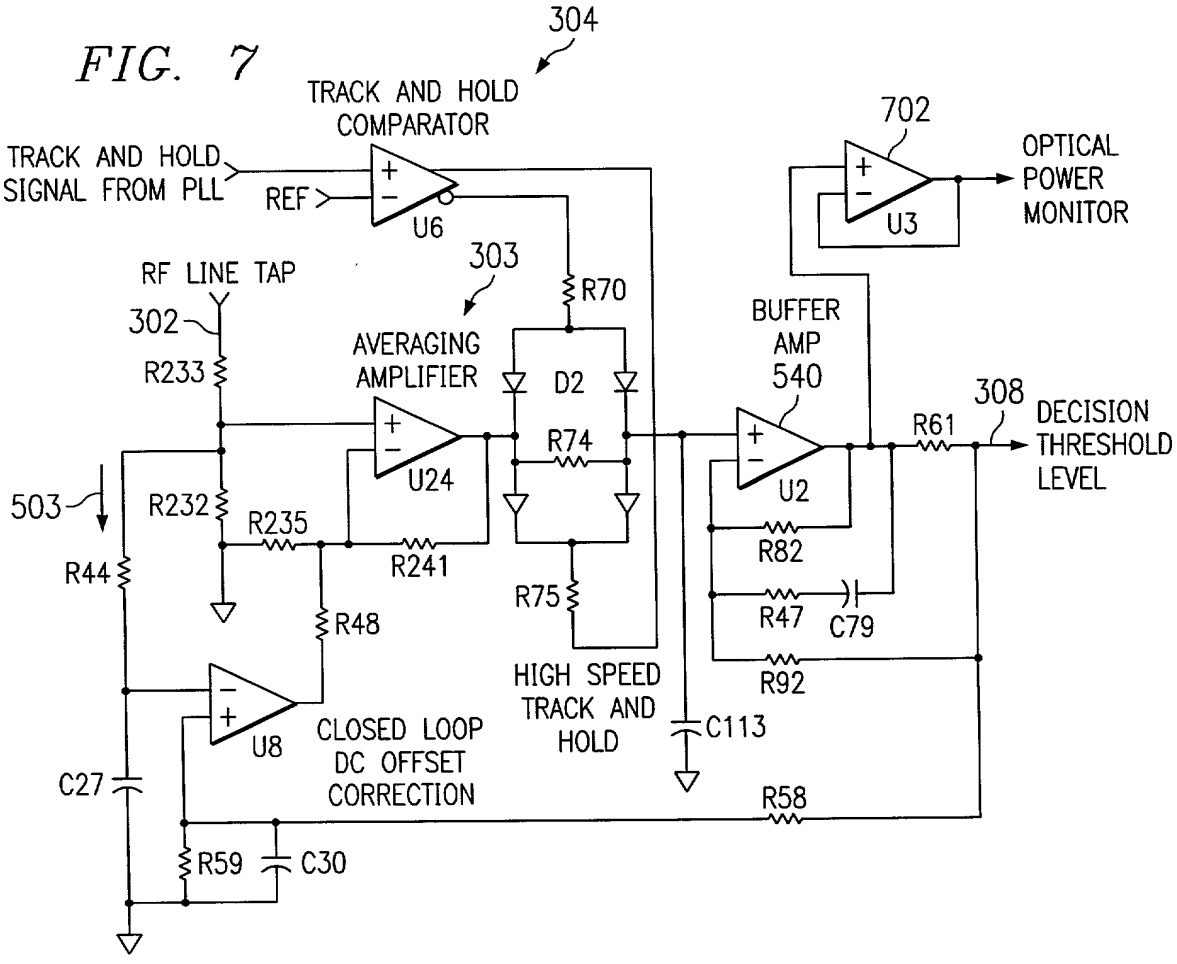

504
U7
RF LINE TAP
302
D4
CLAMPING AMPLIFIER
502
HIGH SPEED CFA AMPLIFIER
506
D3
U1
U23
U7
510
HIGH SPEED PRECISION PEAK DETECTOR
405
SIGNAL TO PLL
U4
305
DARK TIME DETECTOR COMPARATOR

FIG. 7


304
TRACK AND HOLD COMPARATOR
TRACK AND HOLD SIGNAL FROM PLL
REF
U6
702
OPTICAL POWER MONITOR
U3
303
RF LINE TAP
302
R70
BUFFER AMP 540
AVERAGING AMPLIFIER
R233
D2
308
DECISION THRESHOLD LEVEL
R61
U24
R74
U2
503
R232
R235
R82
R44
R241
R75
R47
C79
R48
R92
HIGH SPEED TRACK AND HOLD
U8
CLOSED LOOP DC OFFSET CORRECTION
C113
C27
R58
R59
C30

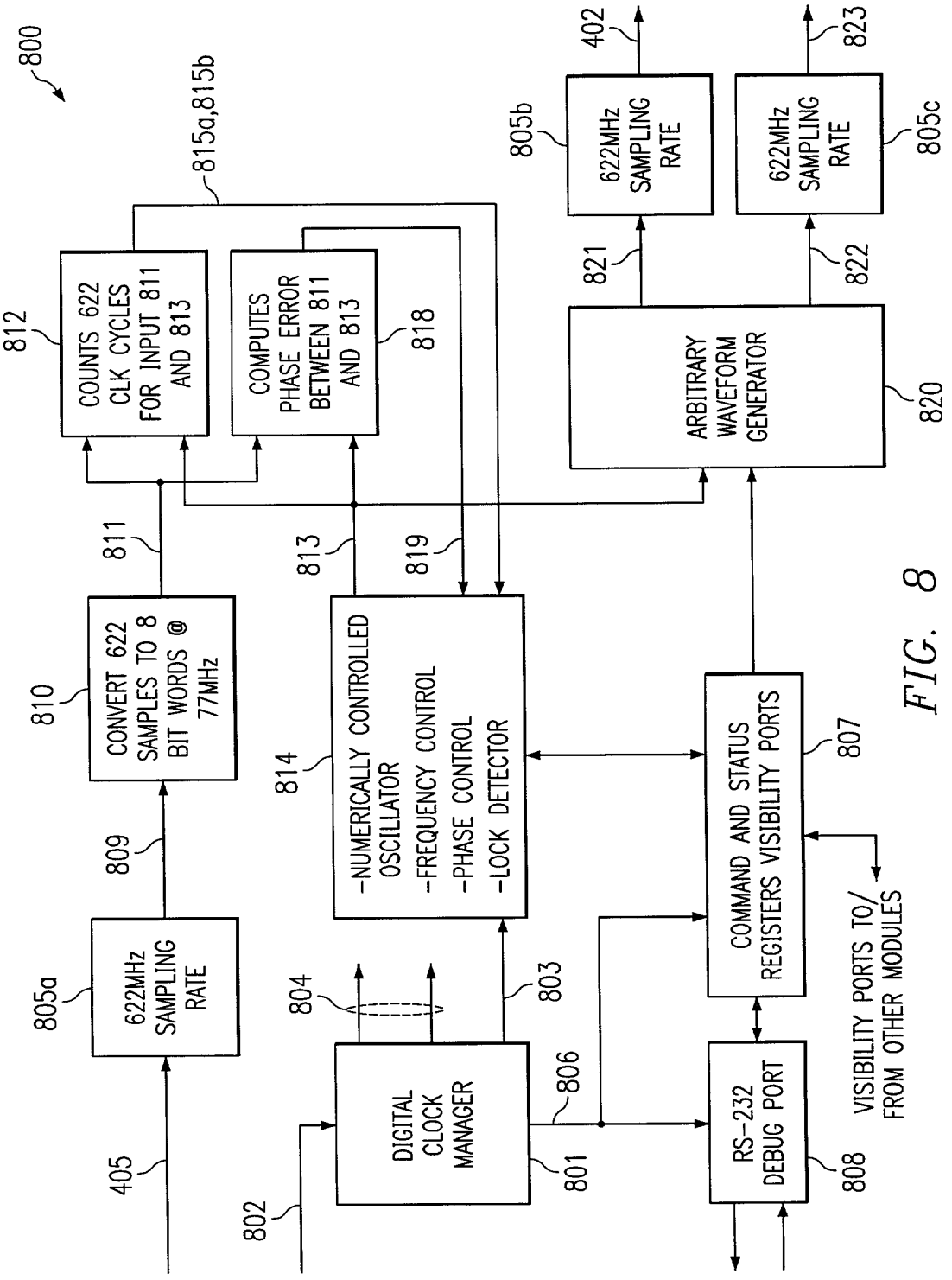

800
815a,815b
812
COUNTS 622 CLK CYCLES FOR INPUT 811 AND 813
COMPUTES PHASE ERROR BETWEEN 811 AND 813
818
805b
622MHz SAMPLING RATE
402
823
622MHz SAMPLING RATE
805c
821
822
ARBITRARY WAVEFORM GENERATOR
820
811
813
819
810
CONVERT 622 SAMPLES TO 8 BIT WORDS @ 77MHz
814
-NUMERICALLY CONTROLLED OSCILLATOR
-FREQUENCY CONTROL
-PHASE CONTROL
-LOCK DETECTOR
COMMAND AND STATUS REGISTERS VISIBILITY PORTS
807
809
805a
622MHz SAMPLING RATE
804
803
806
DIGITAL CLOCK MANAGER
RS-232 DEBUG PORT
808
VISIBILITY PORTS TO/ FROM OTHER MODULES
405
802
801

FIG. 8

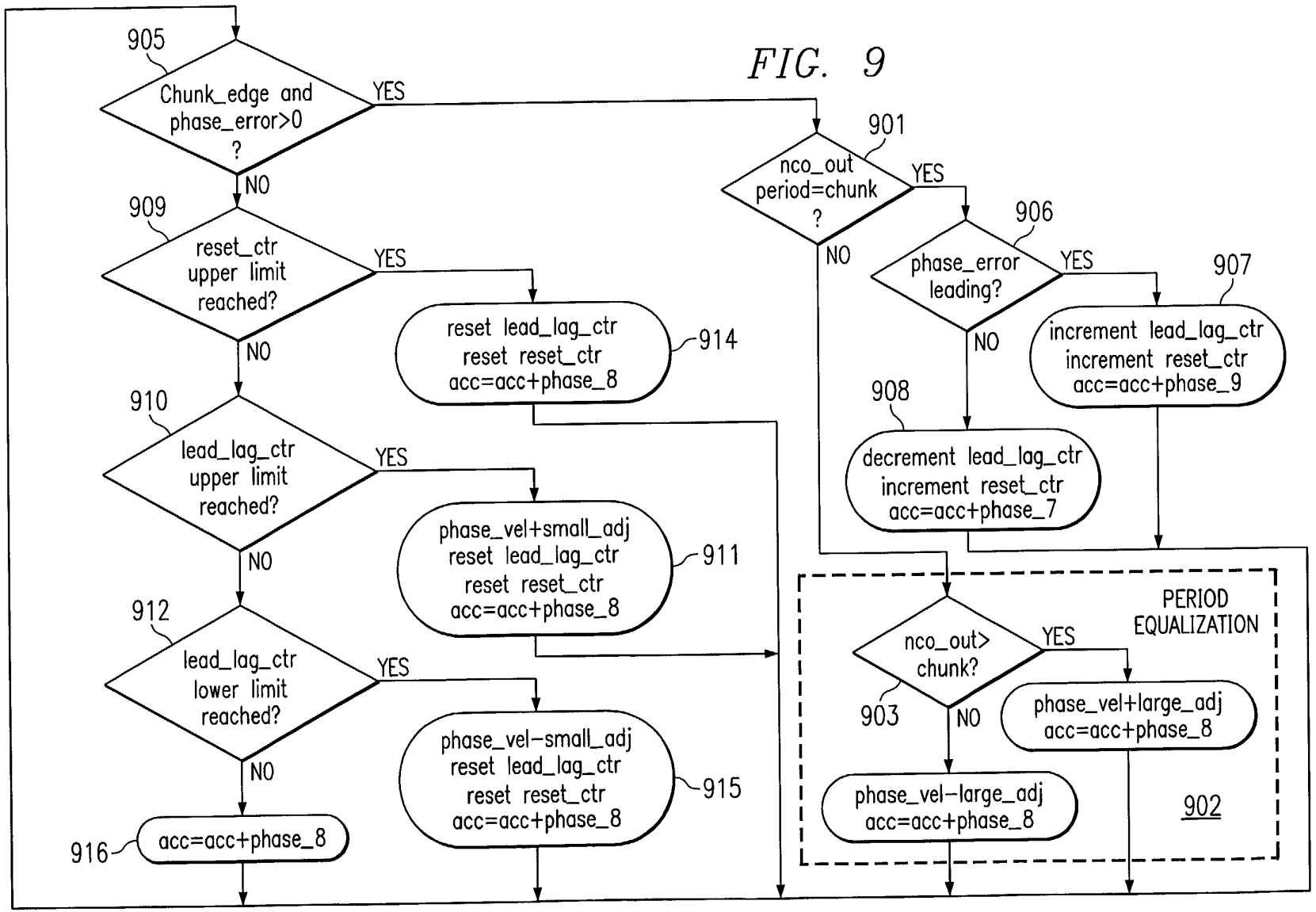


FIG. 9